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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,470	03/09/2000	Hiroshi Katakura	000267	3147

23850 7590 03/23/2005

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/522,470	KATAKURA ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8,13,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7* is/are allowed.

6)☒ Claim(s) *1,2,8,13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 03/02/2005.

2. Claims 1-2, 7-8, 13, and 15-16 are pending in this application. Claims 1-2, 7, 13, and 15-16 are independent claims. In Amendment, claims 1-2, 8, 13, and 15 are amended; claims 3-6, 9-12, and 14 are cancelled; and claim 16 is added. This Office action is made non-final.

Claim Objections

3. Claim 16 is objected to because of the following informalities:

The applicant is advised to re-write the term "CMOS" as "Complementary Metal Oxide Semiconductor (CMOS)" once in claim 16.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 7-8, 13, and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Freeman (Re. 34,363).

Re claim 1, Freeman discloses in Figure 2 a logic circuit comprising: a first inversion section (21) for inverting a first input signal (A) a first logic level and

outputting an inverted first input signal (bar(A)); a second inversion section (22) for inverting a second input signal (B) having a logic level opposite the first logic level and outputting the inverted signal (bar(B)); and a transmission section (transmission lines that connect all signals to 23-26) for receiving the inverted first input signal and the inverted second input signal and outputting one of the inverted first input signal (output controls by C2 and bar(C2)) and the inverted second input signal (output controls by C3 and bar(C3)), wherein the transmission section comprises electrically (e.g. must have current applied in order these logic gates operate in Figure 2) connected transistors (e.g. these OR, AND, XNOR... in Figure 2 must have at least one transistor or in another words, these logic gates are composed of multiple transistors) that respectively receive the inverted first input signal and the inverted second input signal, and the connected transistors output one of the inverted first input signal and the inverted second input signal in response to an externally controllable selection signal (Cs) and an inverted signal of the selection signal (bar(Cs)).

Re claim 2, Freeman discloses in Figure 2 a logic circuit (a portion of Figure 2) comprising a first inversion section (21) for inverting a first input signal (A) and outputting an inverted first input signal (/A); a second inversion section (22) for inverting a second input signal (B) and outputting an inverted second input signal (/B); a first outputting section (output of 25) comprising electrically connected transistors for respectively receiving the inverted first input signal and the inverted second input signal, and the electrically connected transistors one of the inverted first input signal (/A) and the inverted second output signal (/B) in response to an externally controllable first selection

signal (C1) and an inverted signal of the first selection signal (/A); and a second outputting section (output of 24) comprising electrically (e.g. must have current applied in order these logic gates operate in Figure 2) connected transistors for respectively receiving the inverted first input signal and the inverted second input signal, and the electrically connected transistors (e.g. these OR, AND, XNOR... in Figure 2 must have at least one transistor or in another words, these logic gates are composed of multiple transistors) output one of the inverted first input signal and the inverted second input signal in response to an externally controllable second selection signal and an inverted signal of the second selection signal (/B and C3).

Re claim 8, Freeman further discloses in Figure 2 comprising a first switching section (area including transmission lines of A, bar(A) and C2, bar(C2)) provided on an input side of first inversion section (21) and performing switching of whether the first input signal is passed (on) to the first inversion section or blocked (off) in accordance with an external control signal (bar(C2)); and a second switching section (area including transmission lines of B, bar(B) and C3, bar(C3)) provided on an input side of second inversion section (22) and performing switching of whether the second input signal is passed (on) to the second inversion section or blocked (off) in accordance with the external control signal (bar(C3)).

Re claim 13, Freeman further discloses in Figure 2 a first inversion section (21) for inverting a first input signal (21) having one of positive logic and negative logic and outputting an inverted first input signal (bar(A)), first inversion section (21) including transistor circuits (col. 4 lines 45-55) each of transistor circuits having a first input signal

terminal (input of 21) for inputting the first input signal (A), and an outputting terminal (input to 23) for outputting the inverted signal (bar(C2)) based on the logic of the first input signal (A); a second inversion section (22) for inverting a second input signal (B) having negative logic and positive logic, second inversion section (22) including transistor circuits each (col. 4 lines 45-55) of transistor circuits having a second input signal terminal (input to 22) for inputting the second input signal (B), and an outputting terminal (input to 25) for outputting the selection signal (C3) or the inverted signal (bar(C3)) based on the logic of the second input signal; and a transmission section (all the connection bus between inverters to other logic components) for selecting between outputting one of the output of first inversion section (21) and the output of second inversion section (22) in accordance with a logical value which depends upon an externally controllable selection signal (C2 and C3) and an inverted signal of the selection signal (bar(C2) and bar(C3)), transmission selection including transistor circuits (e.g. these OR, AND, XNOR... in Figure 2 must have at least one transistor or in another words, these logic gates are composed of multiple transistors), each of transistor circuits having a first selection signal terminal for inputting the controllable selection signal and a second selection signal terminal for inputting the inverted signal of the selection signal.

Re claim 15, it has similar limitations cited in claim 1. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 16, it has similar limitations cited in claim 13. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 13. Further

Freeman further discloses in Figure 2 these components of circuits are implemented in CMOS (e.g. col. 2 lines 49-55).

Allowable Subject Matter

6. Claim 7 is allowed.

Response to Arguments

7. Applicant's arguments filed 03/02/2005 have been fully considered but they are not persuasive.

a. The applicant argued in page 9 for claim 1 that the transistors are not electrically connected as seen in the reference.

The examiner respectfully submits that the transistors inside the logic gates as OR 23, AND 24, and NOR 26 must electrically connected in order to operate.

b. The applicant argued in page 9 for claim 13 that the cited reference by Freeman does not disclose or suggest the transmission section including transistor circuits wherein each of transistor circuits having a first selection signal terminal for inputting the controllable selection signal and a second selection signal terminal for inputting the inverted signal of the selection signal.

The examiner respectfully submits that Freeman clearly disclose in Figure 2 the transmission section including transistor circuits wherein each of transistor circuits having a first selection signal terminal for inputting the controllable

selection signal and a second selection signal terminal for inputting the inverted signal of the selection signal, for instant the OR 23 circuit has one terminal is connected to the controllable signal bar(C2) and the other terminal is connected to the controllable signal bar(C3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

March 19, 2005

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
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